

FIG. 1



13a(0) WORD LINE DECODER

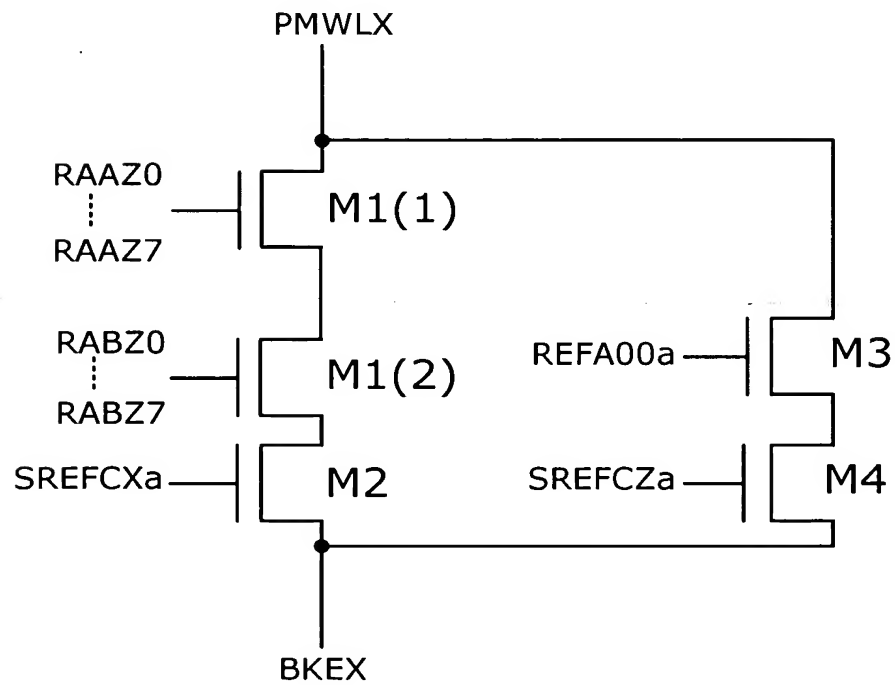


FIG. 3

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT
REGISTER-BASED REFRESH ADDRESS GENERATION
CIRCUIT

Inventor's Name: MORI et al

Application No.: New Application

Docket No.: 108273-00007

19a(1) SHIFT REGISTER

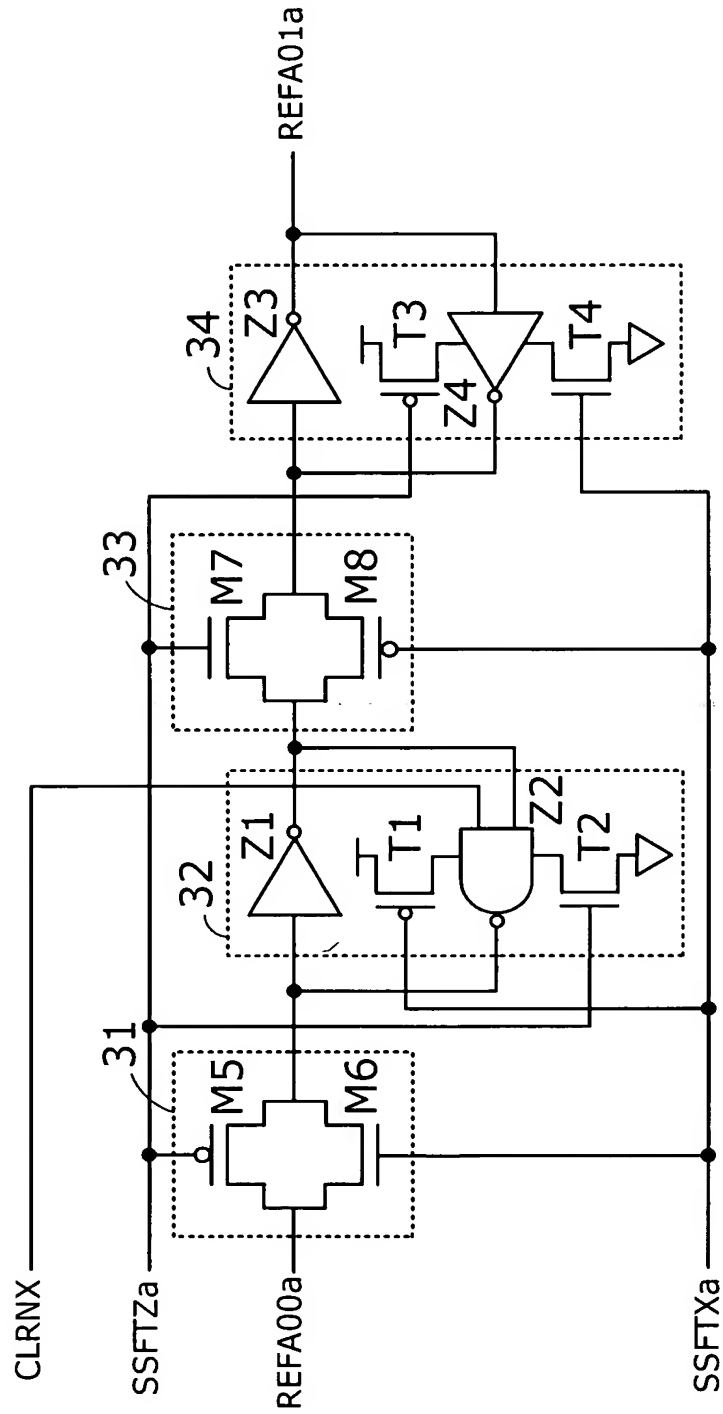


FIG. 4



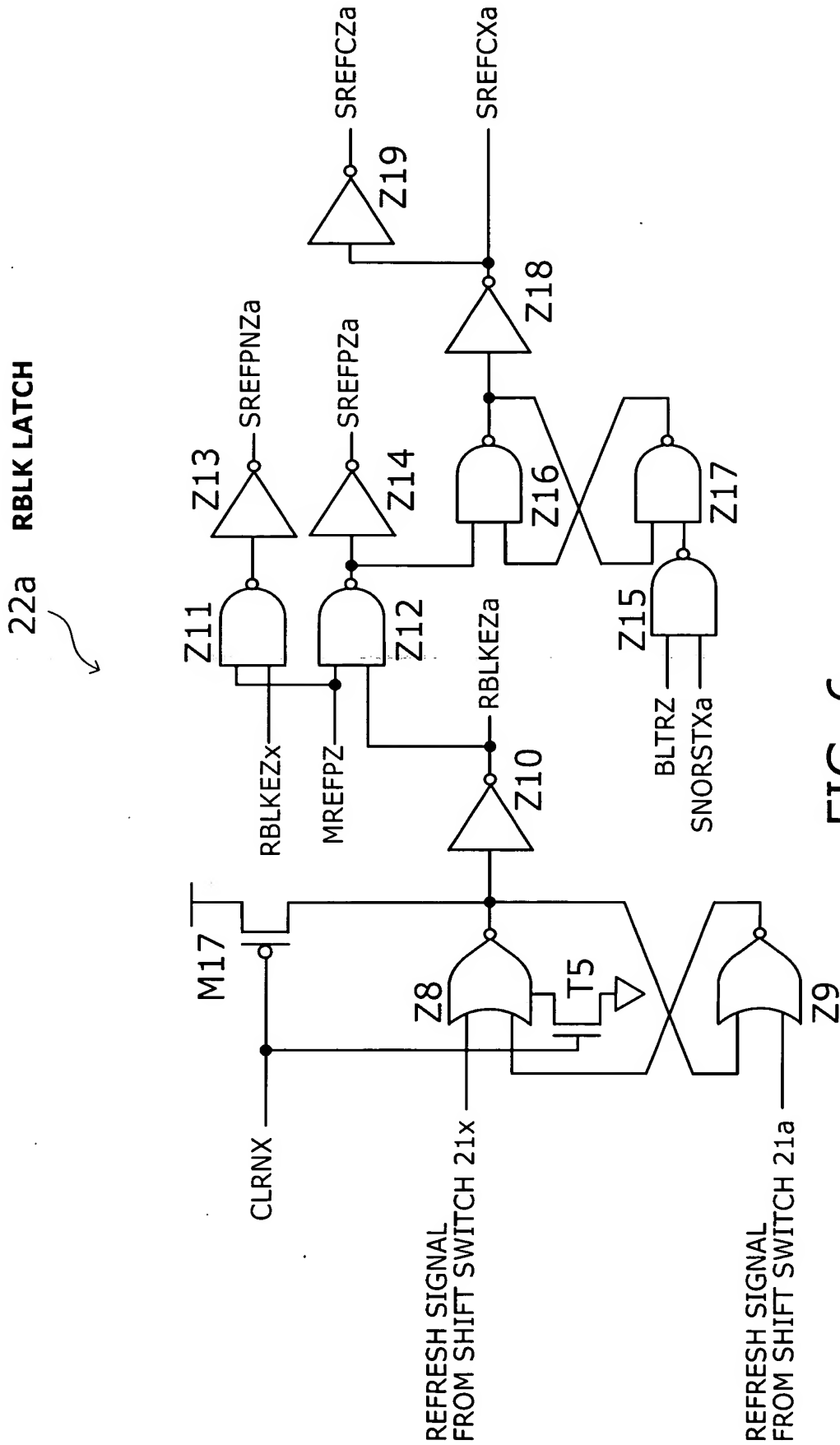


FIG. 6

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT REGISTER-BASED REFRESH ADDRESS GENERATION CIRCUIT

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23a SHIFT COMMAND GENERATOR

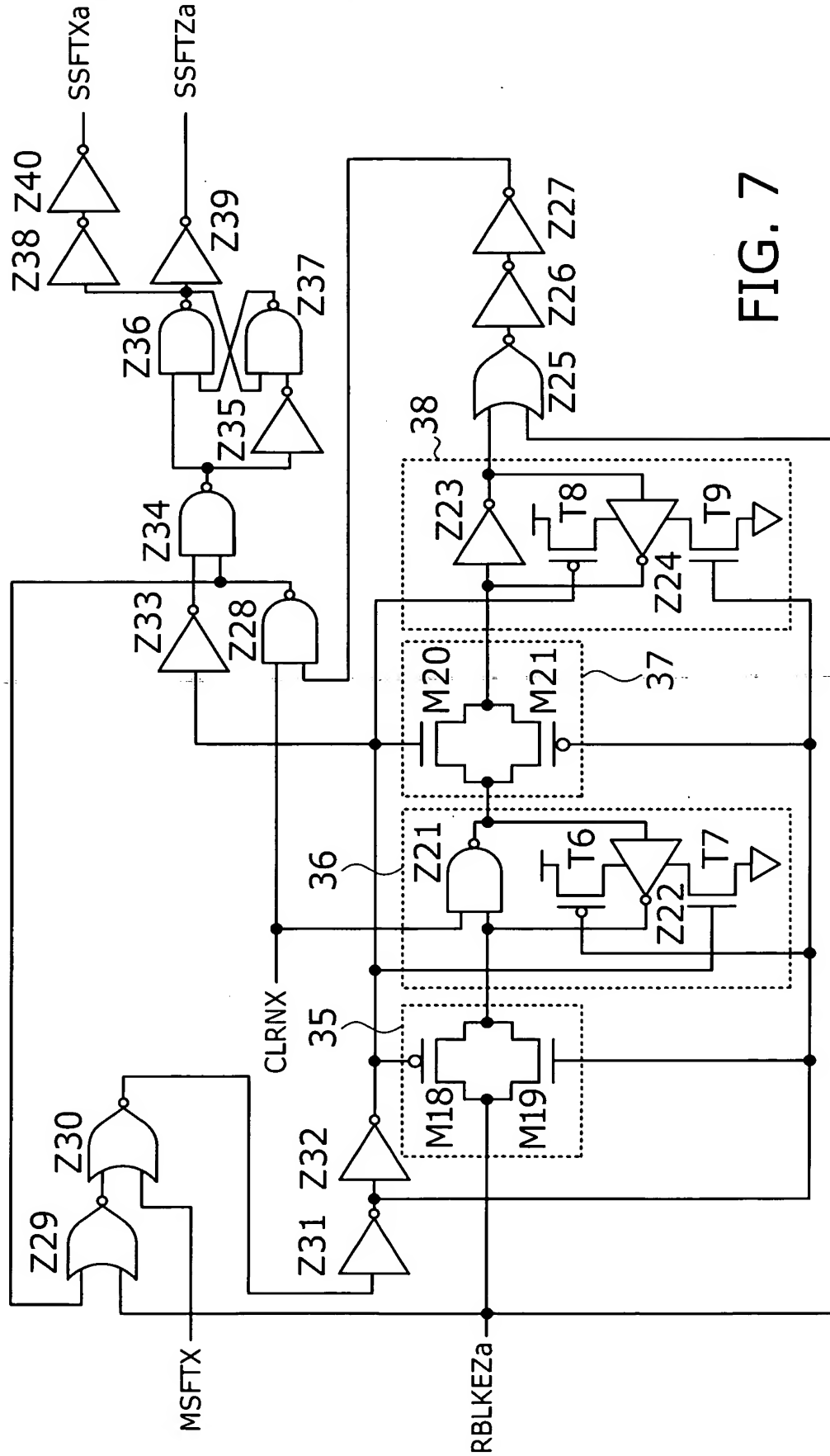


FIG. 7

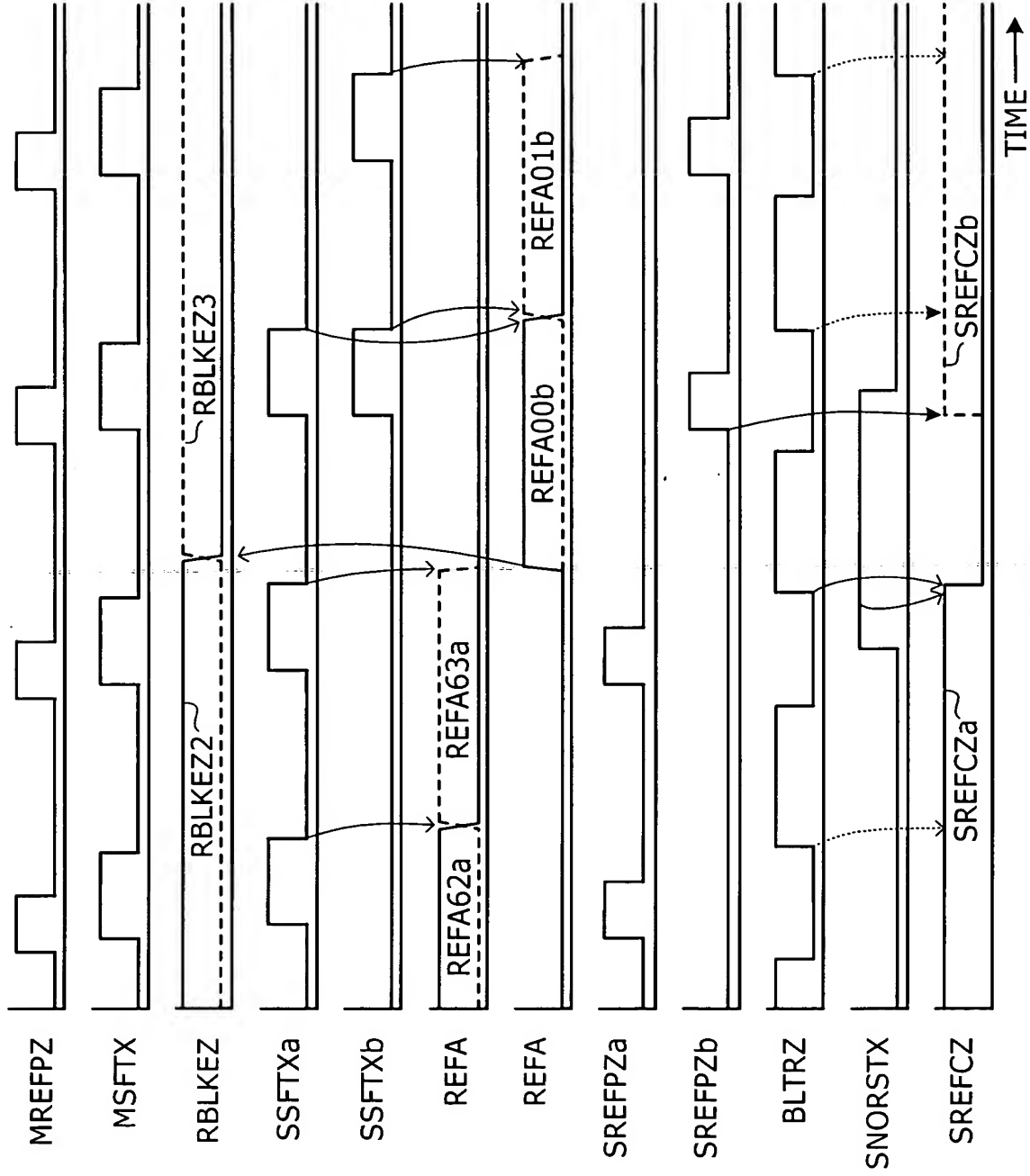


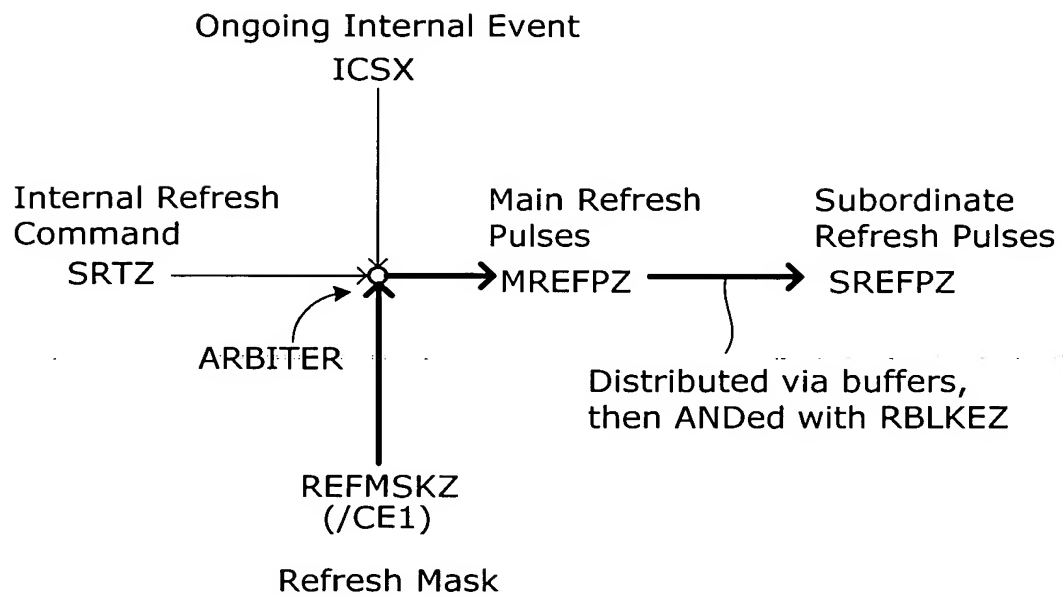
FIG. 8

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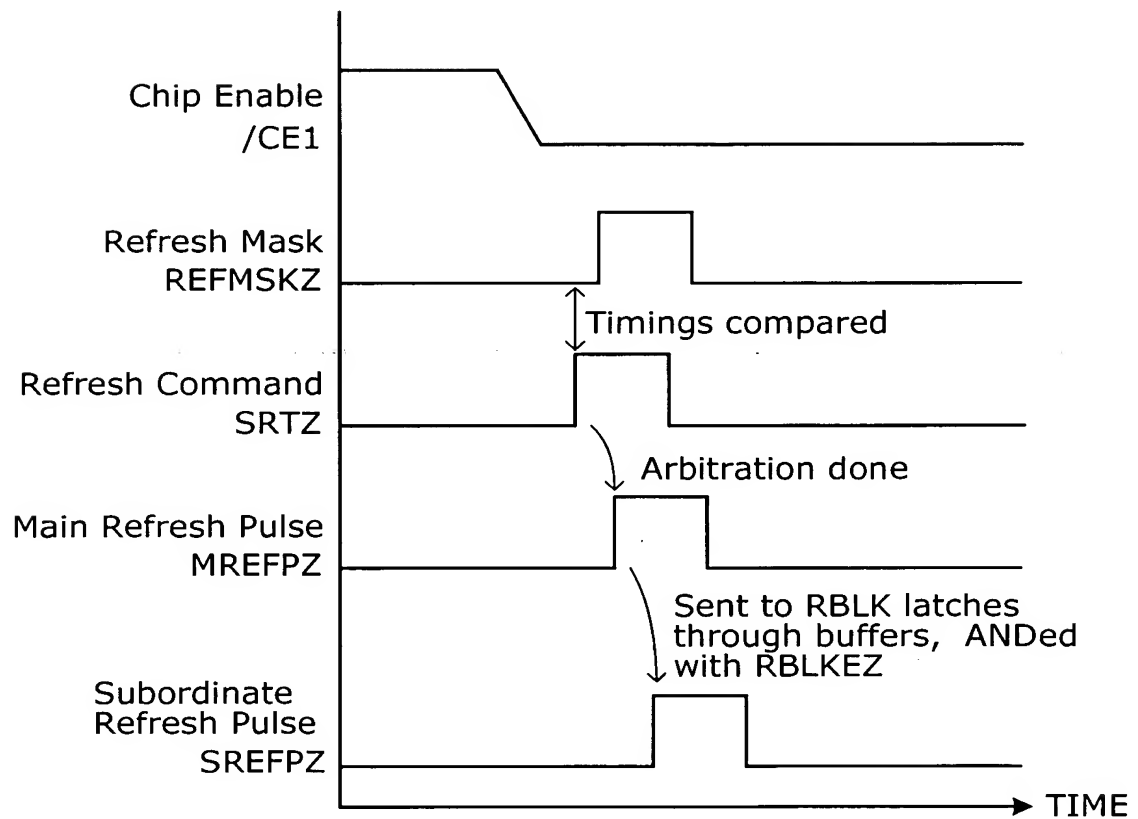
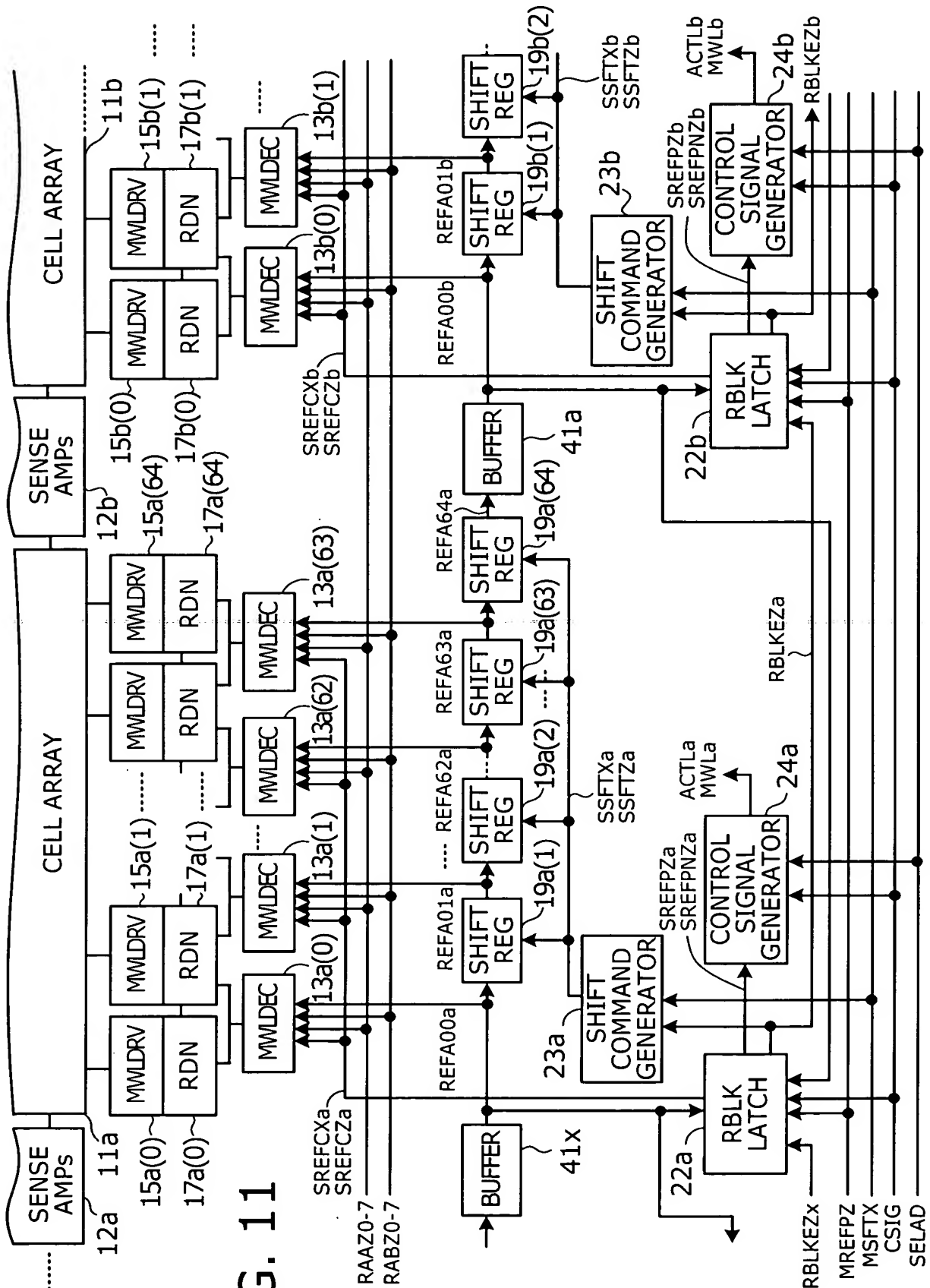


FIG. 10



Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT
REGISTER-BASED REFRESH ADDRESS GENERATION
CIRCUIT

Inventor's Name: MORI et al

Application No.: New Application

Docket No.: 1-8273-00007

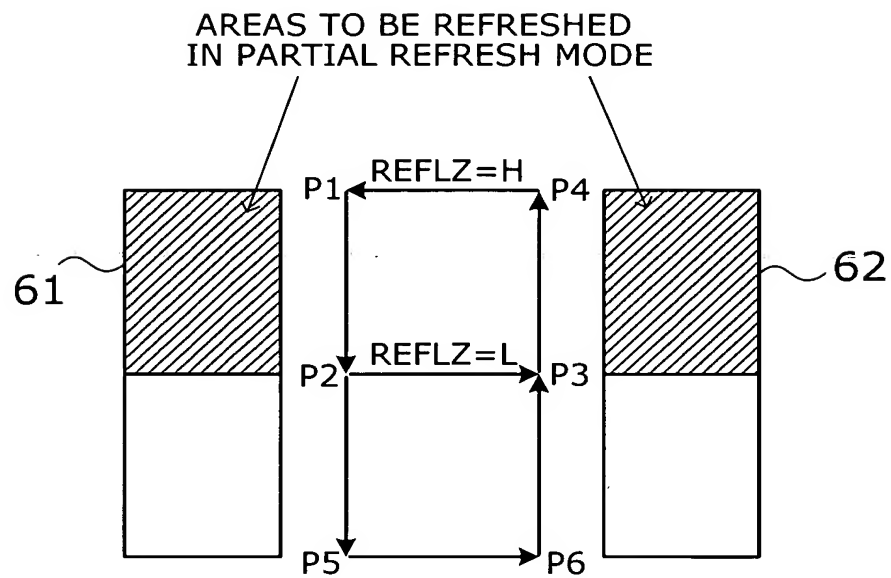


FIG. 13

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT
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Application No.: New Application

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	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1	x1
PARTIAL REFRESH	REFLZ=H (1st)	x1/2	x2
EXIT FROM PARTIAL REFRESH MODE	CE2=H	x1/2	x1/2
EXIT (continued)	REFLZ=H (1st)	x1	x1/2
RETURN TO NORMAL	REFLZ=H (2nd)	x1	x1

FIG. 14

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT
REGISTER-BASED REFRESH ADDRESS GENERATION
CIRCUIT

Inventor's Name: MORI et al

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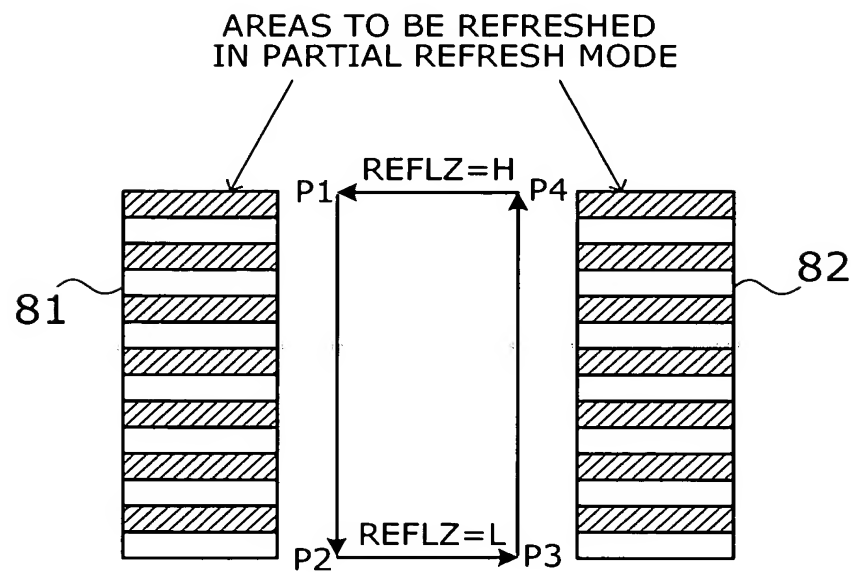


FIG. 16

Title: SEMICONDUCTOR MEMORY DEVICE WITH SHIFT
REGISTER-BASED REFRESH ADDRESS GENERATION
CIRCUIT

Inventor's Name: MORI et al

Application No.: New Application

Docket No.: 108273-00007

	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1	x1
PARTIAL REFRESH	REFLZ=H (1st)	x1/2	x2
EXIT FROM PARTIAL REFRESH MODE (RETURN TO NORMAL)	CE2=H	x1	x1

FIG. 17A

	CONDITION	AREA SIZE	INTERVAL
NORMAL	CE2=H	x1	x1
ENTRY TO PARTIAL REFRESH MODE	CE2=L	x1/2	x1
EXIT FROM PARTIAL REFRESH MODE (RETURN TO NORMAL)	CE2=H	x1	x1

FIG. 17B